Seal Coat

Description

A seal coat is an application of asphalt followed immediately with an aggregate cover. Applications with two layers are referred to as a double chip seal. Rapid-setting asphalt emulsions are normally used when placing a seal coat. Seal coats can waterproof the surface, provide low-severity crack sealing, and restore surface friction.

Timing

You can seal coat at any time in a pavement's life.

Purpose

The primary reason to seal coat an asphalt pavement is to protect the pavement from the deteriorating effects of sun and water. When an asphalt pavement is exposed to sun, wind, and water, the asphalt hardens, or oxidizes. This causes the pavement to become brittle, cracking the pavement. A seal coat provides a waterproof membrane that not only slows down the oxidation process but also helps the pavement shed water, preventing it from entering the base material.

A secondary benefit is an increase in the surface friction, which happens when the cover aggregate adds additional texture to the pavement. A seal coat can increase surface texture on a raveled pavement.

Existing Pavement Condition

Pavements that are dry and raveled are good candidates for seal coating. Some agencies also choose to seal coat pavements in good condition as a preventive maintenance technique.

Maintenance Methods

The Seal Coat Handbook (Mn/DOT document number 1999-07) provides very detailed information about seal coat placement and design.

One of the most important factors when considering a seal coat is the design procedure used to determine the quantities of asphalt binder and cover aggregate. The goal is to have the aggregate particles approximately 70 percent embedded into the asphalt layer. You must make adjustments to account for the traffic volume on the roadway; the absorption of the asphalt binder into the existing pavement; the absorption of the asphalt binder into the cover aggregate; the texture of the existing pavement; and the size, shape, and gradation of the cover aggregate. The correct application rate will result in a single layer of chips embedded approximately 70 percent into the binder with little or no excess chips to remove.